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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/785,604	02/16/2001	Hyun Lee	14-5-3	4376

7590 12/15/2004

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EXAMINER	
DU, THUAN N	
ART UNIT	**PAPER NUMBER**
2116	

DATE MAILED: 12/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/785,604	LEE ET AL.	
	Examiner	Art Unit	
	Thuan N. Du	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,9-13 and 15-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,9-13 and 15-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment (dated 4/28/04).

2. Claims 8 and 14 have been cancelled.

3. Claims 1-7, 9-13 and 15-17 are presented for examination.

4. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Objections

5. Claims 9 and 15 are objected to because of the following informalities: claims 9 and 15 cannot be depended on cancelled claims 8 and 14. For further examination, examiner considers claims 9 and 15 depend on claims 6 and 12 respectively. Appropriate correction is required.

Claim Rejections - 35 USC § 112

6. Claims 9 and 15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

7. Claim 9 recites the limitation "said round trip delay time" in line 1. There is insufficient antecedent basis for this limitation in the claim.

8. Claim 15 recites the limitation "said round trip delay time" in lines 1-2. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

9. Claims 1-7, 9-13 and 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kaplinsky (U.S. Patent No. 5,298,866).

10. **Regarding claim 1**, Kaplinsky teaches a method for distributing a clock signal generated by a clock generator (the clock generator which generates the CLOCK signal shown in Fig. 1) to a plurality of nodes [col. 1, lines 6-9] comprising the steps of:

measuring a clock delay for each of said nodes [col. 2, lines 66-67; col. 5, lines 27-28], wherein said clock delay includes clock generator output delays (fanout) [col. 1, line 62 to col. 2, line 2] and resistive-capacitive (RC) delays [col. 2, lines 8-18]; and

adjusting said clock signal for each node based on said estimated clock delay such that said clock signal arrives at each of said nodes with an aligned phase [col. 2, line 66 to col. 3, line 2; col. 6, line 53 to col. 7, line 2].

Kaplinsky does not explicitly teach that the clock delay is estimated.

However, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Kaplinsky to estimate the clock delay instead of measuring the clock delay because it would allow a faster process of the system.

11. **Regarding claim 2**, Kaplinsky teaches the measuring step further comprises the step of measuring a round trip delay time for the clock signals [col. 3, lines 14-16].

12. **Regarding claim 3**, Kaplinsky teaches that the round trip delay time is obtained using a primary clock path (outward path 15) and a return clock path (return path 29) [Fig. 1; col. 3, lines 17-27; col. 5, lines 29-41].

13. **Regarding claims 4 and 5**, Kaplinsky does not explicitly teach the integrated circuit is a system-on-chip. System-on-chip (SoC) is well known to those of ordinary skill in the art as a chip that integrates microprocessor and all supported components in a single chip. The SoC uses clock distributing network similar to those as the printed circuit board and suffers from similar clock skew problems. Kaplinsky teaches the integrated circuit is a printed circuit board [col. 1, lines 12-16]. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to apply the teachings of Kaplinsky to a system-on-chip to reduce the clock skew associated in such a system.

14. **Regarding claim 6**, Kaplinsky teaches a method for distributing a clock signal generated by a clock generator (the clock generator which generates the CLOCK signal shown in Fig. 1) to a plurality of nodes [col. 1, lines 6-9] comprising the steps of:

providing a feedback clock path for each of said nodes (path 29) [Fig. 1; col. 4, lines 46-49; col. 5, line 29], each of said feedback clock paths having an associated primary clock path that distributes said clock to each node (outward path 15) [Fig. 1; col. 4, lines 50-52; col. 5, lines 29-41];

determining a round trip travel time of said clock signal on each of said primary clock paths and associated feedback clock path [col. 3, lines 14-27];

measuring a clock delay for each of said nodes [col. 2, lines 66-67; col. 5, lines 27-28] using said round trip travel time [col. 3, lines 14-18; col. 5, line 29]; and

adjusting said clock signal for each node based on said estimated clock delay such that said clock signal arrives at each of said nodes with an aligned phase [col. 2, line 66 to col. 3, line 2; col. 6, line 50 to col. 7, line 2].

Kaplinsky does not explicitly teach that the clock delay is estimated.

However, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Kaplinsky to estimate the clock delay instead of measuring the clock delay because it would allow a faster process of the system.

15. **Regarding claim 7** , Kaplinsky teaches that the clock delay includes a clock generator output delays (fanout) [col. 1, line 62 to col. 2, line 2] and a resistive-capacitive (RC) delays [col. 2, lines 8-18].

16. **Regarding claim 9**, Kaplinsky teaches that the round trip delay time is obtained using a primary clock path (outward path 15) and a return clock path (return path 29) [Fig. 1; col. 3, lines 17-27; col. 5, lines 29-41].

17. **Regarding claims 10 and 11**, Kaplinsky does not explicitly teach the integrated circuit is a system-on-chip. System-on-chip (SoC) is well known to those of ordinary skill in the art as a chip that integrates microprocessor and all supported components in a single chip. The SoC uses clock distributing network similar to those as the printed circuit board and suffers from similar clock skew problems. Kaplinsky teaches the integrated circuit is a printed circuit board [col. 1, lines 12-16]. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to apply the teachings of Kaplinsky to a system-on-chip to reduce the clock skew associated in such a system.

18. **Regarding claim 12**, Kaplinsky teaches a network for distributing a clock signal generated by a clock generator (the clock generator which generates the CLOCK signal shown in Fig. 1) to a plurality of nodes [col. 1, lines 6-9] comprising:

a primary clock path that distributes said clock to each node (outward path 15) [Fig. 1; col. 4, lines 46-52];

a feedback clock path associated with each said primary clock paths (return path 29) [Fig. 1; col. 5, lines 29-41];

a phase comparator (phase comparator 63) for determining a round trip travel time of said clock signal on each of said primary clock paths and associated feedback clock path [col. 3, lines 14-16, 28-29; col. 6, lines 43-45]; and

a delay driver (delay element 47 and /or 49) for adjusting said clock signal for each of said nodes based on an measured clock delay for each of said nodes (small, large or the same) based on said round trip travel time [col. 2, lines 66-68; col. 3, lines 14-16; col. 6, line 50 to col. 7, line 2], such that said clock signal arrives at each of said nodes with an aligned phase [col. 2, line 66 to col. 3, line 2].

Kaplinsky does not explicitly teach that the clock delay is estimated.

However, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Kaplinsky to estimate the clock delay instead of measuring the clock delay because it would allow a faster process of the system.

19. **Regarding claim 13**, Kaplinsky teaches that the clock delay includes a clock generator output delays (fanout) [col. 1, line 62 to col. 2, line 2] and a resistive-capacitive (RC) delays [col. 2, lines 8-18].

20. **Regarding claim 15**, Kaplinsky teaches that the round trip delay time is obtained using a primary clock path (outward path 15) and a return clock path (return path 29) [Fig. 1; col. 3, lines 17-27; col. 5, lines 29-41].

21. **Regarding claims 16 and 17**, Kaplinsky does not explicitly teach the integrated circuit is a system-on-chip. System-on-chip (SoC) is well known to those of ordinary skill in the art as a chip that integrates microprocessor and all supported components in a single chip. The SoC uses clock distributing network similar to those as the printed circuit board and suffers from similar clock skew problems. Kaplinsky teaches the integrated circuit is a printed circuit board [col. 1, lines 12-16]. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to apply the teachings of Kaplinsky to a system-on-chip to reduce the clock skew associated in such a system.

Conclusion

22. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thuan N. Du whose telephone number is (571) 272-3673. The examiner can normally be reached on Monday and Wednesday-Friday: 10:00 AM - 8:30 PM, EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne H. Browne can be reached on (571) 272-3670.

Central TC telephone number is (571) 272-2100.

The fax number for the organization is (703) 872-9306.

23. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll free).

Thuan N. Du
December 3, 2004